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Intrinsic Response Time of Normally Off MESFET's of GaAs, Si, and InP

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Invited Paper

***Abstract*—A response time of normally off MESFET's for high-speed logic circuits made of GaAs, Si, and InP was calculated using a two-dimensional numerical analysis. The results indicate that GaAs is the best material among them. The step response of the InP FET is not as fast as expected from v/E characteristics due to low electric field in the channel for low-power logic operation of a normally off FET.**

I. Introduction

RECENTLY, GaAs MESFET's have been actively used for high-speed logic circuits. Using a normally on FET, a propagation delay per gate (t_{pd}) of 34 ps with a dissipation power (P_{dis}) of 41 mW was obtained [1]. For normally off FET's, 77 ps of t_{pd} with 977 μW of P_{dis} has been achieved [2], and 72 ps with 890 μW as the latest data [3]. From these experimental results, the superiority of GaAs to Si as basic material has been made clear. Since t_{pd} of several tens picoseconds has been achieved, it is significant to estimate an intrinsic response time (t_{int}) of the FET itself.

In this paper, t_{int} for normally off MESFET's made of GaAs, Si, and InP have been calculated using a two-dimensional numerical analysis and the results compared.

Manuscript received July 24, 1979; revised January 10, 1980.
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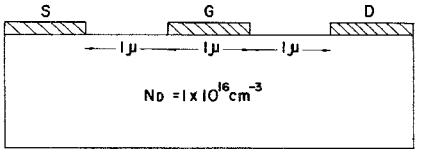

Fig. 1. The two-dimensional analytical model for MESFET.

II. Analytical Model

A model for the analysis is a two-dimensional planar type MESFET with an n-type active layer as shown in Fig. 1. For the convenience of simplicity of the calculation, a semi-insulating substrate is not considered. The donor concentration is 1×10^{16} cm^{-3}. The gate length (l_g) is 1 μm and the source–drain distance is 3 μm. Basic equations are as follows:

$$-\nabla^2\varphi = q/\epsilon\cdot(N_D - n) \tag{1}$$

$$\partial n/\partial t = \nabla(n\cdot v + D\cdot\nabla n) \tag{2}$$

$$\nabla J_{tot} = \nabla(q\cdot n\cdot v + q\cdot D\cdot\nabla n + \epsilon\cdot\partial E/\partial t) = 0 \tag{3}$$

where φ is the potential, q is the electronic charge, ϵ is the dielectric constant, n is the electron density, E is the electric field, v is the drift velocity, and D is the diffusivity. In order to solve these equations, the Successive-Over-Relaxation method was used for Poisson's equation (1) and the Successive-Under-Relaxation method was

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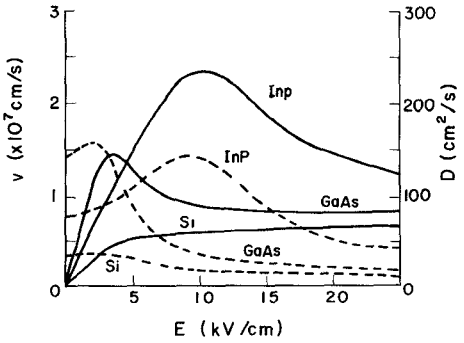

Fig. 2. The v/E and D/E characteristics of GaAs, Si, and InP. The solid lines describe the velocity and the broken lines the diffusivity.

TABLE I
DEVICE PARAMETERS

	Dielectric constant ϵ_s	Impurity density N_D cm^{-3}	Active layer thickness t_{epi} μm	Schottky barrier height ϕ_{BN} V	Mobility μ $cm^2V^{-1}s^{-1}$
GaAs	12.53	$1x10^{16}$	0.35	0.8	5500
Si	11.80	$1x10^{16}$	0.35	0.8	1350
InP	12.37	$1x10^{16}$	0.28	0.5	3000

used for the time variant continuity equation (2). The device current was obtained from (3) for the gate width of 10 μm (W_g). The mesh is 100×15. In this analysis, the minority hole carrier current and avalanche multiplication are ignored.

Device parameters for the calculation are listed in Table I. An active layer thickness t_{epi} of the GaAs FET was determined by the two-dimensional analysis on the assumption that the depletion layer just pinches off the channel at $V_{GS}=0$ V. The t_{epi} of the Si FET is much the same as that for the GaAs FET because of nearly equal Schottky barrier heights ϕ_{BN} and dielectric constants ϵ_s. In the case of the InP FET, t_{epi} is set to be $\sqrt{0.5/0.8}\times0.35=0.277$ μm reflecting the difference in ϕ_{BN}. The dependencies of the velocities and the diffusivities on electric field are shown in Fig. 2, [4]–[6]. These curves correspond to an impurity concentration of $N_D=1\times10^{16}$ cm^{-3} (300 K). In our model, diffusivities are assumed to be isotropic and velocity overshoot is neglected.

III. Calculation Results

The static characteristics for the various cases are illustrated in Fig. 3. In the "off" state when $V_{GS}=0$ V, the drain current I_D of the three FET's are almost zero.

In the time-variant analysis, the intrinsic response time of the FET itself may be defined as the time needed for a 90-percent change in I_D from I_{on} to I_{off} and vice versa, resulting from the abrupt switching of V_{GS} under constant V_{DS} [7]. In Fig. 4 the transient calculation result for the GaAs FET is shown for l_g as the parameter and constant t_{epi}. It is seen that the "off" drain current I_{off} strongly depends on the l_g in spite of the same t_{epi}. Reducing the gate length has the same tendency as increasing t_{epi} as shown in Fig. 5 for $l_g=1$ μm. That is, I_D becomes large

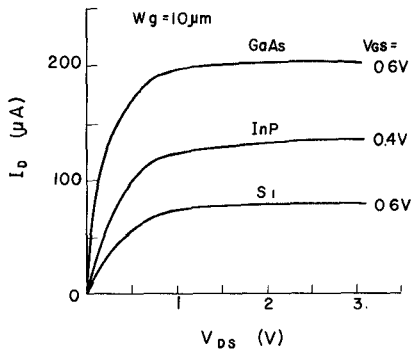

Fig. 3. The static characteristics of the normally off FET's.

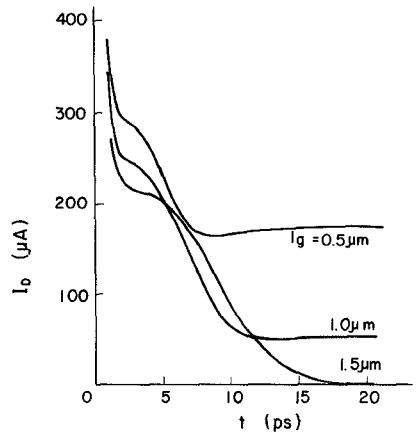

Fig. 4. The step response of the GaAs FET. The parameter is a gate length (l_g). The t_{epi} is 0.4 μm. V_{GS} switches from 0.6 to 0.1 V at $V_{DS}=0.8$ V.

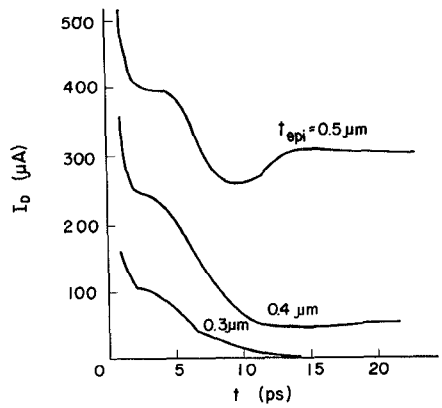

Fig. 5. The step response of the GaAs FET. The parameter is an active layer thickness (t_{epi}). The l_g is 1 μm. V_{GS} switches from 0.6 to 0.1 V at $V_{DS}=0.8$ V.

and t_{int} becomes small as the gate is shortened. The reason for this tendency can not be explained by a one-dimensional model and it is considered to be a two-dimensional effect. As shown in Fig. 6, depletion-layer depth and resulting channel height varies with gate length l_g. Selection for normally off MESFET should be done based on the gate length l_g.

The transient calculation results for GaAs, Si, and InP FET's being switched from "on" to "off" are shown in Fig. 7. In this case, for the GaAs and Si FET's, V_{GS} changes from 0.6 to 0 V instantaneously at $V_{DS}=0.8$ V, and for InP from 0.4 to 0 V at $V_{DS}=0.5$ V at time=0.

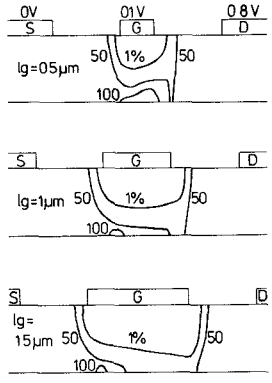

Fig. 6. The electron concentration profiles for the "off" steady-state ($t = 50$ ps) in Fig. 4.

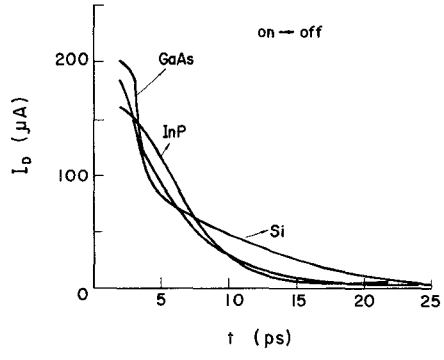

Fig. 7. The step response of the normally off FET's for different materials.

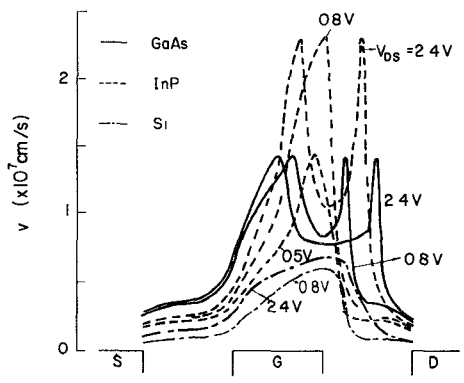

Fig. 8. The velocity profiles of the normally off FET's at "on" state.

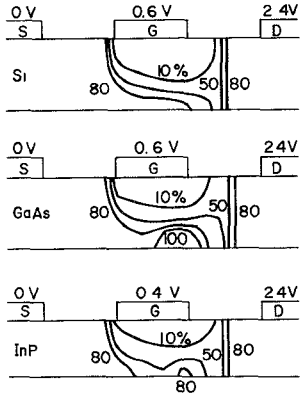

Fig. 9. The electron concentration profiles of the normally off FET's.

TABLE II
CALCULATED RESULTS OF THE INTRINSIC RESPONSE TIME OF THE NORMALLY OFF MESFET'S. W_g IS 10 μm

	V_{DS} V	V_{GS} V	I_{on} μA	I_{off} μA	t_{on} ps	t_{off} ps	P_{dis}* μW
GaAs	0.8	0-0.6	194.3	3.5	12.4	10.4	79
Si	0.8	0-0.6	71.2	1.1	22.1	21.3	29
InP	0.5	0-0.4	107.4	2.5	16.8	14.0	28

*$P_{dis} = V_{DS} \cdot (I_{on}+I_{off})/2$

Here, V_{DS} is set to be the built-in potential of the Schottky gate. t_{off} is 10.4 ps for GaAs, 21.3 ps for Si and 14.0 ps for InP. Thus t_{int} of the three FET's is in the order GaAs < InP < Si even in the case of "off"→"on" as listed in Table II.

The calculated velocity profiles at the bottom of the channel are illustrated in Fig. 8. At high drain voltage ($V_{DS} = 2.4$ V), the average velocity $\bar{v}$ of InP is larger than that of GaAs [8], because of the higher peak velocity and the relatively flat v/E curve for InP as shown in Fig. 2. Since the $\bar{v}$ of Si in the active channel region is less than half of GaAs and InP, the channel transit time of Si is largest among the three materials. In addition, because of low mobility in the ohmic region between the source and the gate, the Si FET is the slowest. The velocity dropback near the gate edge at the drain side was seen both in GaAs with V_{DS} higher than 0.8 V and InP with V_{DS} higher than 2.4 V. The velocity dropback was accompanied by the formation of a high-field region in which electron accumulation occurs as shown in Fig. 9. Since the active layer of the GaAs FET is thicker than that of the InP FET, electrons accumulate more in GaAs than in InP. It is expected that the InP FET will be able to operate at higher frequency and will have a higher switching speed than a GaAs FET in the case of normally on logic operation with high drain voltage.

On the other hand, for the logic circuits using a normally off FET, V_{DS} is clamped at approximately the barrier height of the Schottky gate of the following FET stage as previously mentioned. At such low V_{DS}, the maximum field in the channel is several kV/cm and exceeds the GaAs peak field (~3.5 kV/cm) but not the InP peak field (~10 kV/cm). Therefore, the transit time of the InP is estimated to be longer than that of GaAs, because the $\bar{v}$ of InP at $V_{DS} = 0.5$ V is smaller than that of GaAs at $V_{DS} = 0.8$ V in the region under the gate and between the gate and drain. Moreover, in the ohmic region between the source and the gate, since the electron mobility for InP is about half of that for GaAs, the series resistance R_{SG} may be larger for InP than for GaAs. Consequently the intrinsic response time of InP normally off MESFET's is larger than for GaAs.

IV. CONCLUSION

The intrinsic step response time of the normally off MESFET was calculated from a two-dimensional numerical analysis for the three materials GaAs, Si, and InP. GaAs has the shortest switching time among them. The

response of the InP FET is not as fast as expected from its v/E curve, because the operating drain voltage is relatively small in the normally off FET and the maximum electric field in the channel is less than the 10-kV/cm value required for the InP drift velocity to reach its peak.

To improve the response time of the InP FET, a p-n junction FET or a short-gate FET with $l_g \cong 0.5$ μm is a possibility since it would result in a larger channel field.

Acknowledgment

The authors express their thanks to K. Kurumada and T. Mizutani for useful discussions and M. Watanabe, Y. Sato, and M. Fujimoto for their encouragement.

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Determination of the Electrode Capacitance Matrix for GaAs FET's

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***Abstract*—In this paper, a method is presented which provides the electrode capacitance matrix for GaAs FET's. The method incorporates a Green's function, valid for conductors printed on or embedded in a grounded substrate, with the moment method technique. Although calculations for various geometries of printed conductors are considered, emphasis is placed on the computation of self- and mutual-capacitances for the source, gate, drain equivalent circuit of a GaAs FET. As an example, the speed power characteristics of a depletion-mode GaAs FET inverter circuit are examined, as a function of device width, pad and gate length.**

I. Introduction

IN THIS PAPER, an accurate model is developed for the determination of the capacitance matrix of multiple conductors with finite dimensions, printed on or embedded in a grounded dielectric substrate. This model has applications in the optimization of high speed integrated circuits (IC's) for which a precise knowledge of the capacitance matrix for the electrodes is of paramount importance for the device and IC design. In order to maximize the speed and minimize the power of the IC, the electrode capacitance matrix must be computed as a function of device width, contact and gate length. By incorporating this capacitance model in the computer-aided design program SPICE2, the speed–power tradeoff of a GaAs FET inverter circuit has been analyzed, as a function of device dimensions, in order to demonstrate the model's usefulness.

The method given here allows for the computation of the capacitance matrix of a system of N, zero thickness, metallic conductors with finite dimensions (see Fig. 1). The approach utilizes the moment methods technique [1] in conjunction with a Green's function appropriate to the geometry of the problem. In this manner, by employing even–odd mode excitations, the unknown charge on each conductor can be determined, which immediately yields the capacitance matrix. The potential V_i of the ith conductor being known, $i=1,2,3,\cdots,N$ the problem is to solve the following system of integral equations

$$V_i = \sum_{j=1}^{N} \int_{S_j} G\{x_i,y_i;x_j,y_j;z\}\,\sigma_j(x_j,y_j)\,dx_j\,dy_j \qquad (1)$$

Manuscript received June 15, 1979; revised February 20, 1980. This work was supported in part by the Avionics Laboratory Air Force Systems Command, Wright-Patterson AFB, OH, under Contract No. F33615-76-C-1214, Lutz Micheel contract monitor.

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